Microprocessor Systems

Code	Credit Hours
EE-222	3-1

COURSE DESCRIPTION:

The course covers the architectural aspects and assembly language programming of general purpose processors based on RISC (ARM, MIPS, RISC-V, etc) architecture. The course also includes the study of one of the micro-controllers architecture (AVR, PIC, ARM Cortex M, etc) and developing real-time applications with them. The skills acquired can be used in the areas of electronics, communications, embedded system and industrial automation design.

TEXTBOOK:

1. The AVR Microcontroller and Embedded Systems: Using Assembly and C by Mazidi et al., Prentice Hall
2. Computer Organization and Design The Hardware/Software Interface (RISC-V Edition) by Hennessy and Patterson, Morgan Kaufmann

REFERENCE BOOK:

1. Some Assembly Required; Assembly language programming with the AVR microcontroller by Margush, CRC
2. Definitive Guide to the ARM Cortex-M3 and M4 Microcontrollers, Third Edition by Joseph Yiu.

PREREQUISITES

Nil

ASSESSMENT SYSTEM FOR THEORY

Quizzes	5-15%
Assignments	5-10%
Mid Terms	25-35%
ESE	40-50%

ASSESSMENT SYSTEM FOR LAB

Quizzes	10%-15%
Assignments	5% - 10%
Lab Work and Report	70-80%
Lab ESE/Viva/Project	20-30%

TEACHING PLAN

WEEK NO	TOPICS	LEARNING OUTCOMES
1	Introduction	Course Outline, objectives, teaching plan, assessment method, Introduction to Computing Systems
2-4	AVR Microcontrollers (Basics)	Introduction to AVR Microcontrollers, AVR architecture, AVR Assembly Language (Load and Store Addressing Modes, Arithmetic Operation, Flags, Jumps and Branches, Procedure Calls and Stack, Bit Operations)
5-8	AVR Microcontroller (Advance)	AVR Internal Memory Manipulation, AVR Timers, AVR interrupts, AVR Programming in C, AVR Serial Port and C Programming
9	**MID TERM EXAM**	
10-11	AVR Microcontroller (Advance)	AVR Sensor Interfacing, AVR ADC, AVR Pulse Width Modulation, AVR DC Motor Control, AVR SPI & I2C
12-17	RISC V	Introduction RISC-V Architecture, RISC-V Assembly Introduction, RISC-V Logical Operations, RISC-V Instructions for Making Decisions, RISC-V Supporting Procedures in Computer Hardware, RISC-V Instruction Formats, RISC-V Addressing for Wide Immediates and Addresses, RISC-V, Translating and Starting a Program, Future Directions in Computing
18	**END SEMESTER EXAMS**	

Lab Experiments:

NO	DESCRIPTION
1	Intro to AVR Programming, Simulation and Hardware Implementation
2	Memory, Arithmetic and Logical Operations (Part I)
3	Memory, Arithmetic and Logical Operations (Part II)
4	Memory Instructions and Branches
5	Functions & Delays
6	Digital Input Output
7	AVR C Programming
8	Timer Programming
9	AVR Interrupts (Timer Interrupts)
10	AVR Hardware Interrupts
11	AVR Serial Communication
12	Voltmeter Design (Open Ended Lab)
13	RISC-V Assembly (Part I: Introduction)
14	RISC-V Assembly (Part II)
15	RISC-V Assembly (Part III)